

Serial No. 10/797,081

Attorney Docket No. 01-592-RCE

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device having a plurality of thin film resistance element elements located above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance element elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°, wherein each of the plurality of thin film resistance elements has a similar shape.

2. (Currently Amended) The semiconductor device according to claim 1, wherein the interlayer insulating film comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the plurality of thin film resistance element elements is formed.

3. (Currently Amended) The semiconductor device according to claim 1, wherein the interlayer insulating film comprises an inorganic spin-on-glass film, and wherein an upper surface of the interlayer insulating film has a higher area adjacent to an area where the plurality of thin film resistance element elements is formed than in the area where the plurality of thin film resistance element elements is not formed.

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4. (Currently Amended) The semiconductor device according to claim 1, wherein the plurality of thin film resistance element elements is formed on an area where the wire is formed, and a wire interval is set to 1.7 μ m or more.

5. (Currently Amended) The semiconductor device according to claim 1, wherein the plurality of thin film resistance element elements is formed above the area where the wire is formed, and the plurality of thin film resistance element elements and the wire are disposed in parallel to each other so that projections thereof are overlapped with each other.

6. (Currently Amended) A semiconductor device having a plurality of thin film resistance element elements located above an interlayer insulating film above an area where at least one of an element and a wire is formed, wherein the interlayer insulting film comprises an inorganic spin-on-glass film formed so as to cover the overall area below an area where the plurality of thin film resistance element elements is formed, wherein each of the plurality of thin film resistance elements has a similar shape.

7. (Withdrawn) A method of manufacturing the semiconductor device of claim 6, the method comprising:

rotationally coating an inorganic spin-on-glass film to form the inorganic spin-on-glass film as the interlayer insulating film above the area while flattening the upper surface of the inorganic spin-on-glass film; and

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forming any one of the thin film resistance element and an insulating film constituting the interlayer insulating film on the inorganic spin-on-glass film flattened by the rotational coating.

8. (Withdrawn) A method of manufacturing a semiconductor device having a thin film resistance element through an interlayer insulating film above an area where at least one of an element and a wire is formed, the method comprising:

rotationally coating an inorganic spin-on-glass film to form the inorganic spin-on-glass film as the interlayer insulating film above the area while flattening the upper surface of the inorganic spin-on-glass film; and

forming any one of the thin film resistance element and an insulating film constituting the interlayer insulating film on the inorganic spin-on-glass film flattened by the rotational coating.

9. (Currently Amended) A semiconductor device having a plurality of thin film resistance element elements disposed above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance element elements is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film formed so as to cover the overall area below the area where the thin film resistance element is formed, wherein the plurality of thin film resistance element elements is formed on an area where the wire is formed, and a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape.

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10. (Currently Amended) The semiconductor device according to claim 9, wherein each of the plurality of thin film resistance element elements is formed to have a width in a range between 1 and 10 μ m, and a thickness in a range between 10 and 50nm.

11. (Currently Amended) The semiconductor device according to claim 3, wherein each of the plurality of thin film resistance element elements is formed to have a width in a range between 1 and 10 μ m, and a thickness in a range between 10 and 50nm.

12. (Currently Amended) A semiconductor device having a plurality of thin film resistance element elements disposed above an interlayer insulating film above an area where a plurality of wires is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance element elements is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film, wherein a wire interval is set to 1.7 μ m or more, wherein each of the plurality of thin film resistance elements has a similar shape.

13. (Currently Amended) The semiconductor device according to claim 1, wherein the plurality of thin film resistance element elements further comprises paired thin film resistance elements.

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14. (Currently Amended) The semiconductor device according to claim 1, ~~further comprising a plurality of the thin film resistance element, wherein the area~~ areas where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements ~~[[is]]~~ are identical.

15. (Currently Amended) The semiconductor device according to claim 1, ~~wherein the thin film resistance element further comprises paired thin film resistance elements, wherein the area~~ areas where at least one of the element and the wire is formed below each of the paired thin film resistance elements ~~[[is]]~~ are identical.

16. (New) The semiconductor device according to claim 1, wherein each of the plurality of thin film resistance elements comprises chromium silicon.

17. (New) The semiconductor device according to claim 6, wherein each of the plurality of thin film resistance elements comprises chromium silicon.